

What is claimed is:

- 1 1. A printed circuit board having a surface providing a mating interface to which is
- 2 electrically connected an electrical connector having signal conductors and ground
- 3 conductors, the printed circuit board comprising:
 - 4 a plurality of stacked dielectric layers, with a conductor disposed on at least one
 - 5 of the plurality of dielectric layers;
 - 6 the mating interface including:
 - 7 a plurality of conductive vias aligned in a plurality of rows, the plurality of
 - 8 conductive vias extending through at least a portion of the plurality of dielectric
 - 9 layers, at least one of the plurality of conductive vias intersecting the conductor;
 - 10 the plurality of conductive vias including signal conductor connecting
 - 11 conductive vias and ground conductor connecting conductive vias; and
 - 12 for each of the plurality of rows of the conductive vias, there are at least
 - 13 twice as many ground conductor connecting conductive vias as signal conductor
 - 14 connecting conductive vias and the conductive vias are positioned relative to one
 - 15 another so that for each signal conductor connecting conductive via, there are
 - 16 ground conductor connecting conductive vias adjacent either side of the signal
 - 17 conductor connecting conductive via.

- 1 2. The printed circuit board of claim 1, wherein a distance between a signal
- 2 conductor connecting conductive via and an adjacent ground conductor connecting

3 conductive via of a row is less than a distance between adjacent rows of the conductive
4 vias.

1 3. The printed circuit board of claim 1, wherein for each of the plurality of rows of
2 the conductive vias, a distance between a signal conductor connecting conductive via and
3 an adjacent ground conductor connecting conductive via on one side is similar to a
4 distance between the signal conductor connecting conductive via and an adjacent ground
5 conductor connecting conductive via on the other side.

1 4. The printed circuit board of claim 1, which further comprises a surface mounting
2 pad disposed on each of the plurality of conductive vias, the signal conductors and
3 ground conductors of the electrical connector being electrically connected to the surface
4 mounting pads.

1 5. The printed circuit board of claim 4, wherein the surface mounting pad
2 corresponding to each signal conductor connecting conductive via is substantially
3 configured in an I-shape and the surface mounting pads corresponding to adjacent ground
4 conductor connecting conductive vias are substantially configured in an H-shape.

1 6. The printed circuit board of claim 1, which further comprises:
2 a ground plane layer through which at least some of the plurality of conductive
3 vias extend; and

4 for each signal conductor connecting conductive via of the ground plane layer,
5 there is provided an area surrounding the signal conductor connecting conductive via that
6 is free of the ground plane layer.

1 7. The printed circuit board of claim 6, wherein for each ground conductor
2 connecting conductive via of the ground plane layer, there is provided at least one
3 discrete area adjacent the ground conductor connecting conductive via that is free of the
4 ground plane layer.

1 8. The printed circuit board of claim 1, which further comprises:
2 a power voltage plane layer through which at least some of the plurality of
3 conductive vias extend; and
4 for each signal conductor connecting conductive via and its corresponding
5 adjacent ground conductor connecting conductive vias extending through the power
6 voltage plane layer, there is provided an area surrounding the conductive vias that is free
7 of the power voltage plane layer.

1 9. A printed circuit board having a surface providing a mating interface to which is
2 electrically connected an electrical connector having signal conductors and ground
3 conductors, the printed circuit board comprising:
4 a plurality of stacked dielectric layers;
5 the mating interface including:

6 a plurality of conductive vias aligned in a plurality of rows, the plurality of
7 conductive vias extending through at least a portion of the plurality of dielectric
8 layers;

9 the plurality of conductive vias including signal conductor connecting
10 conductive vias and ground conductor connecting conductive vias; and
11 for each of the plurality of rows of the conductive vias, each signal
12 conductor connecting conductive via has corresponding ground conductor
13 connecting conductive vias adjacent either side of the signal conductor connecting
14 conductive via so as to form a repeating pattern along the row of ground
15 conductor connecting conductive via - signal conductor connecting conductive via
16 - ground conductor connecting conductive via.

1 10. The printed circuit board of claim 9, wherein a distance between a signal
2 conductor connecting conductive via and an adjacent ground conductor connecting
3 conductive via of a row is less than a distance between adjacent rows of the conductive
4 vias.

1 11. The printed circuit board of claim 9, wherein for each of the plurality of rows of
2 the conductive vias, a distance between a signal conductor connecting conductive via and
3 an adjacent ground conductor connecting conductive via on one side is similar to a
4 distance between the signal conductor connecting conductive via and an adjacent ground
5 conductor connecting conductive via on the other side.

1 12. The printed circuit board of claim 9, which further comprises a surface mounting
2 pad disposed on each of the plurality of conductive vias, the signal conductors and
3 ground conductors of the electrical connector being electrically connected to the surface
4 mounting pads.

1 13. The printed circuit board of claim 12, wherein the surface mounting pad
2 corresponding to each signal conductor connecting conductive via is substantially
3 configured in an I-shape and the surface mounting pads corresponding to adjacent ground
4 conductor connecting conductive vias are substantially configured in an H-shape.

1 14. The printed circuit board of claim 9, which further comprises:
2 a ground plane layer through which at least some of the plurality of conductive
3 vias extend; and
4 for each signal conductor connecting conductive via of the ground plane layer,
5 there is provided an area surrounding the signal conductor connecting conductive via that
6 is free of the ground plane layer.

1 15. The printed circuit board of claim 14, wherein for each ground conductor
2 connecting conductive via of the ground plane layer, there is provided at least one
3 discrete area adjacent the ground conductor connecting conductive via that is free of the
4 ground plane layer.

1 16. The printed circuit board of claim 9, which further comprises:

2 a power voltage plane layer through which at least some of the plurality of
3 conductive vias extend; and
4 for each signal conductor connecting conductive via and its corresponding
5 adjacent ground conductor connecting conductive vias extending through the power
6 voltage plane layer, there is provided an area surrounding the conductive vias that is free
7 of the power voltage plane layer.

1 17. A printed circuit board having a surface providing a mating interface to which is
2 electrically connected an electrical connector having signal conductors and ground
3 conductors, the printed circuit board comprising:
4 a plurality of stacked dielectric layers;
5 the mating interface including:
6 a plurality of conductive vias aligned in a plurality of interleaved first and
7 second rows, the plurality of conductive vias extending through at least a portion
8 of the plurality of dielectric layers;
9 the plurality of conductive vias including signal conductor connecting
10 conductive vias and ground conductor connecting conductive vias; and
11 for each of the plurality of first rows, each signal conductor connecting
12 conductive via has corresponding ground conductor connecting conductive vias
13 adjacent either side of the signal conductor connecting conductive via so as to
14 form a repeating pattern along the row of ground conductor connecting
15 conductive via - signal conductor connecting conductive via - ground conductor
16 connecting conductive via;

17 for each of the plurality of second rows, each signal conductor connecting
18 conductive via has corresponding ground conductor connecting conductive vias
19 adjacent either side of the signal conductor connecting conductive via so as to
20 form a repeating pattern along the row of ground conductor connecting
21 conductive via - signal conductor connecting conductive via - ground conductor
22 connecting conductive via; and
23 the positions of the signal conductor connecting conductive vias in the
24 first rows relative to the positions of the signal conductor connecting conductive
25 vias in the second rows are offset so that each signal conductor connecting
26 conductive via in the first and second rows has a ground conductor connecting
27 conductive via adjacent at least three sides.

1 18. The printed circuit board of claim 17, wherein for each of the plurality of first and
2 second rows of the conductive vias, a distance between a signal conductor connecting
3 conductive via and an adjacent ground conductor connecting conductive via on one side
4 is similar to a distance between the signal conductor connecting conductive via and an
5 adjacent ground conductor connecting conductive via on the other side.

1 19. The printed circuit board of claim 17, which further comprises a surface mounting
2 pad disposed on each of the plurality of conductive vias, the signal conductors and
3 ground conductors of the electrical connector being electrically connected to the surface
4 mounting pads.